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Endian-safe record representation clauses for Ada programs

Relevance scale

Mike Mardis

December 1999 ACM SIGAda Ada Letters, Volume XIX Issue 4

Publisher: ACM Press

Full text available: Tpdf(294.44 KB)

Additional Information: full citation, index terms

W. Hollingsworth, H. Sachs, A. J. Smith

February 1989 Communications of the ACM, Volume 32 Issue 2

2 The Clipper processor: instruction set architecture and implementation

Publisher: ACM Press

Full text available: pdf(4.67 MB) Additional Information: full citation, abstract, references, citings,

index terms, review

Intergraph's CLIPPER microprocessor is a high performance, three chip module that implements a new instruction set architecture designed for convenient programmability, broad functionality, and easy future expansion.

3 An unconventional proposal: using the x86 architecture as the ubiquitous

virtual standard architecture

Jochen Liedtke, Nayeem Islam, Trent Jaeger, Vsevolod Panteleenko, Yoonho Park September 1998 Proceedings of the 8th ACM SIGOPS European workshop on Support for composing distributed applications EW 8

Publisher: ACM Press

Full text available: T pdf(410.74

KB)

Additional Information: full citation, index terms

4 Wholesale byte reversal of the outermost Ada record object to achieve

endian independence for communicated data types

Randal P. Andress

September 2005 ACM SIGAda Ada Letters, Volume XXV Issue 3

Publisher: ACM Press

Full text available: T pdf(143.50 KB)

Additional Information: full citation, abstract, index terms

For years computer engineers have dealt with the problems associated with transfer of binary data between systems of different bit and byte order. Big-Endian (most significant first) vs. Little-Endian (least significant first). In this article, existing techniques are extended to develop a new, systematic method for coding Ada record component representations so that the same declaration may be used to define an input/output object of a communications link (or "flat" file) to achieve complete en ...

5 Extensions for multi-module records in conventional programming languages



D. R. Cheriton, M. E. Wolf

October 1987 Proceedings of the 14th ACM SIGACT-SIGPLAN symposium on Principles of programming languages POPL '87

Publisher: ACM Press

Full text available: Top pdf(1.19 MB) Additional Information: full citation, abstract, references, citings,

index terms

An extended record facility is described that supports multi-module records by providing: incremental and distributed record type definition, allowing field names of a record to be declared in different modules with different subscopes relative to the root record declaration. field-level declaration of access to records by modules and procedures, specification of record representation in terms of the underlying computer memor ...

Reverse interpretation + mutation analysis = automatic retargeting





Christian S. Collberg

May 1997 ACM SIGPLAN Notices, Proceedings of the ACM SIGPLAN 1997 conference on Programming language design and implementation PLDI '97, Volume 32 Issue 5

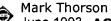
Publisher: ACM Press

Full text available: pdf(1.92 MB) Additional Information: full citation, abstract, references, citings,

There are three popular methods for constructing highly retargetable compilers:

- (1) the compiler emits abstract machine code which is interpreted at run-time,
- (2) the compiler emits C code which is subsequently compiled to machine code by the native C compiler, or (3) the compiler's code-generator is generated by a back-end generator from a formal machine description produced by the compiler writer. These methods incur high costs at run-time, compile-time, or compiler-construction time, respectiv ...
- 7 Usenet nuggets





June 1993 ACM SIGARCH Computer Architecture News, Volume 21 Issue 3

Publisher: ACM Press

Full text available: T pdf(325.50

KB)

Additional Information: full citation, index terms

8 The SimpleScalar tool set, version 2.0



Doug Burger, Todd M. Austin

June 1997 ACM SIGARCH Computer Architecture News, Volume 25 Issue 3

Publisher: ACM Press

Full text available: pdf(985.46 KB)

Additional Information: full citation, abstract, citings, index terms

This document describes release 2.0 of the SimpleScalar tool set, a suite of free, publicly available simulation tools that offer both detailed and high-performance simulation of modern microprocessors. The new release offers more tools and capabilities, precompiled binaries, cleaner interfaces, better documentation, easier installation, improved portability, and higher performance. This paper contains a complete description of the tool set, including retrieval and installation instructions, a d ...

9 A new page table for 64-bit address spaces

M. Talluri, M. D. Hill, Y. A. Khalidi

December 1995 ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles SOSP '95, Volume 29 Issue 5

Publisher: ACM Press

Full text available: pdf(1.97 MB) Additional Information: full citation, references, citings, index terms

10 Software engineering: applications, practices and tools (SE): NextGen





eXtreme porting: structured by automation

Pradeep Varma, Ashok Anand, Donald P. Pazel, Beth R. Tibbitts

March 2005 Proceedings of the 2005 ACM symposium on Applied computing SAC '05

Publisher: ACM Press

Full text available: pdf(282.44 Additional Information: full citation, abstract, references, index terms

"Maintenance is really the normal state of an XP project" - Beck. Thus porting is a natural candidate for eXtreme Programming and we present a novel tool-based XP methodology for porting C/C++ programs. The structure provided by our tooling is designed for scalability, to enable XP on large projects porting enterprise-scale codebases. Overall planning and iteration planning of the methodology are assisted by a novel, first-of-its-kind migration orchestrator tool. Automated test, debugging, and a ...

Keywords: XP, analyze, debug, dialects, eXtreme programming, fix, orchestration, port planning, re-factor, software process model, test

11 Software issues: Control flow based obfuscation



Jun Ge, Soma Chaudhuri, Akhilesh Tyagi

November 2005 Proceedings of the 5th ACM workshop on Digital rights management DRM '05

Publisher: ACM Press

Full text available: pdf(316.58 Additional Information: full citation, abstract, references, index terms

A software obfuscator is a program O to transform a source program P for protection against malicious reverse engineering. O should be correct (O(P) has same functionality with P), resilient (O(P) is resilient against attacks), and effective (O(P) is not too much slower than P). In this paper we describe the design of an obfuscator which consists of two parts. The first part extracts the control flow information from the program and ...

Keywords: control flow, software obfuscation

12 Distributed systems - programming and management: On remote procedure call



Patrícia Gomes Soares

November 1992 Proceedings of the 1992 conference of the Centre for Advanced Studies on Collaborative research - Volume 2 CASCON '92

Publisher: IBM Press

Full text available: R pdf(4.52 MB) Additional Information: full citation, abstract, references, citings

The Remote Procedure Call (RPC) paradigm is reviewed. The concept is described, along with the backbone structure of the mechanisms that support it. An overview of works in supporting these mechanisms is discussed. Extensions to the paradigm that have been proposed to enlarge its suitability, are studied. The main contributions of this paper are a standard view and classification of RPC mechanisms according to different perspectives, and a snapshot of the paradigm in use today and of goals for t ...

13 FLIP: an internetwork protocol for supporting distributed systems



M. Frans Kaashoek, Robbert van Renesse, Hans van Staveren, Andrew S. Tanenbaum

February 1993 ACM Transactions on Computer Systems (TOCS), Volume 11 Issue 1

Publisher: ACM Press

Full text available: pdf(2.29 MB) Additional Information: full citation, abstract, references, citings, index terms

Most modern network protocols give adequate support for traditional applications such as file transfer and remote login. Distributed applications, however, have different requirements (e.g., efficient at-most-once remote procedure call even in the face of processor failures). Instead of using ad hoc protocols to meet each of the new requirements, we have designed a new protocol, called the Fast Local Internet Protocol (FLIP), that provides a clean and simple integrated approach to these new ...

14 Space efficient conservative garbage collection



Hans-Juergen Boehm

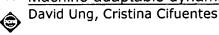
June 1993 ACM SIGPLAN Notices, Proceedings of the ACM SIGPLAN 1993 conference on Programming language design and implementation PLDI '93, Volume 28 Issue 6

Publisher: ACM Press

Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, references, citings, index terms

We call a garbage collector conservative if it has only partial information about the location of pointers, and is thus forced to treat arbitrary bit patterns as though they might be pointers, in at least some cases. We show that some very inexpensive, but previously unused techniques can have dramatic impact on the effectiveness of conservative garbage collectors in reclaiming memory. Our most significant observation is that static data that appears to point to the heap should not result i ...

15 Machine-adaptable dynamic binary translation



January 2000 ACM SIGPLAN Notices, Proceedings of the ACM SIGPLAN workshop on Dynamic and adaptive compilation and optimization DYNAMO '00, Volume 35 Issue 7

Publisher: ACM Press

Full text available: pdf(1.23 MB) Additional Information: full citation, abstract, references, citings, index terms

Dynamic binary translation is the process of translating and optimizing executable code for one machine to another at runtime, while the program is "executing" on the target machine.

Dynamic translation techniques have normally been limited to two particular machines; a competitor's machine and the hardware manufacturer's machine. This research provides for a more general framework for dynamic translations, by providing a framework based on specifications of machines that ...

Keywords: binary translation, dynamic compilation, dynamic execution, emulation, interpretation

16 Intrusion detection and prevention: On deriving unknown vulnerabilities from





zero-day polymorphic and metamorphic worm exploits

Jedidiah R. Crandall, Zhendong Su, S. Felix Wu, Frederic T. Chong
November 2005 Proceedings of the 12th ACM conference on Computer and
communications security CCS '05

Publisher: ACM Press

Full text available: pdf(334.95 Additional Information: full citation, abstract, references, index terms

Vulnerabilities that allow worms to hijack the control flow of each host that they spread to are typically discovered months before the worm outbreak, but are also typically discovered by third party researchers. A determined attacker could discover vulnerabilities as easily and create zero-day worms for vulnerabilities unknown to network defenses. It is important for an analysis tool to be able to generalize from a new exploit observed and derive protection for the vulnerability. Many researcher ...

Keywords: honeypots, metamorphism, polymorphic worms, polymorphism, symbolic execution, worms

17 Exploiting recursion to simplify RPC communication architectures





D. R. Cheriton

August 1988 ACM SIGCOMM Computer Communication Review , Symposium proceedings on Communications architectures and protocols SIGCOMM '88, Volume 18 Issue 4

Publisher: ACM Press

Full text available: pdf(1.64 MB) Additional Information: full citation, abstract, references, citings, index terms

Current communication architectures suffer from a growing collection of protocols in the host operating systems, gateways and applications, resulting in increasing implementation and maintenance cost, unreliability and difficulties with interoperability. The remote procedure call (RPC) approach has been used in some distributed systems to contain the diversity of application layer protocols within the procedure call abstraction. However, the same technique cannot be applied ...

18 Improving the efficiency of the OSI checksum calculation





October 1989 ACM SIGCOMM Computer Communication Review, Volume 19

Issue 5

Publisher: ACM Press

Full text available: pdf(629.71 KB)

Additional Information: full citation, abstract, citings, index terms

It is known that using larger byte--sizes to access memory usually results in faster computations of checksum algorithms. This paper proposes two different ways to use larger byte--sizes to improve the performance of the OSI checksum. First, an algorithm is presented that computes the 8--bit checksum using 16-bit integers. It is shown that this algorithm yields a 5 to 20 percent performance improvement on many architectures. Second, the benefits of expanding the basic computation unit of the OSI ...

19 Linux Network Programming, Part 1

Ivan Griffin, John Nelson

February 1998 Linux Journal

Publisher: Specialized Systems Consultants, Inc.

Full text available: html(18.70 Additional Information: full citation, abstract, references, index terms

BSD Sockets: This is the first of a series of articles about how to devlop networked applications using the various interfaces available on Linux

20 The KScalar simulator



J. C. Moure, Dolores I. Rexachs, Emilio Luque

March 2002 **Journal on Educational Resources in Computing (JERIC)**, Volume 2 Issue 1

Publisher: ACM Press

Full text available: pdf(493.35 Additional Information: full citation, abstract, references, index terms

Modern processors increase their performance with complex microarchitectural mechanisms, which makes them more and more difficult to understand and evaluate. KScalar is a graphical simulation tool that facilitates the study of such processors. It allows students to analyze the performance behavior of a wide range of processor microarchitectures: from a very simple in-order, scalar pipeline, to a detailed out-of-order, superscalar pipeline with non-blocking caches, speculative execution, and comp ...

Keywords: Education, pipelined processor simulator

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1 Platform independent translations for a Compilable Ada Abstract Syntax

Warren D. Ferguson, John K. Whiteman

October 1993 Proceedings of the conference on TRI-Ada '93 TRI-Ada '93

Publisher: ACM Press

Full text available: 🔁 pdf(1.08 MB) Additional Information: full citation, references, index terms

2 Alpha AXP architecture

Richard L. Sites

February 1993 Communications of the ACM, Volume 36 Issue 2

Publisher: ACM Press

Full text available: pdf(4.62 MB) Additional Information: full citation, references, citings, index

terms, review

Keywords: Alpha AXP chip

3 Optimising hot paths in a dynamic binary translator

David Ung, Cristina Cifuentes

March 2001 ACM SIGARCH Computer Architecture News, Volume 29 Issue 1

Publisher: ACM Press

Full text available: pdf(890.10

Additional Information: full citation, abstract, citings, index terms

In dynamic binary translation, code is translated "on the fly" at run-time, while the user perceives ordinary execution of the program on the target machine. Code fragments that are frequently executed follow the same sequence of flow control over a period of time. These fragments form a hot path and are optimised to improve the overall performance of the program. Multiple hot paths may also exist in programs. A program may choose to execute in one hot path for some time, but later switch to anot ...

Keywords: binary translation, dynamic compilation, dynamic execution, run-time profiling

Machine-adaptable dynamic binary translation

David Ung, Cristina Cifuentes

January 2000 ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN workshop on Dynamic and adaptive compilation and optimization DYNAMO '00, Volume 35 Issue 7

Publisher: ACM Press

Full text available: 🔁 pdf(1.23 MB) Additional Information: full citation, abstract, references, citings, index terms

Dynamic binary translation is the process of translating and optimizing executable code for one machine to another at runtime, while the program is "executing" on the target machine.

Dynamic translation techniques have normally been limited to two particular machines; a competitor's machine and the hardware manufacturer's machine. This research provides for a more general framework for dynamic translations, by providing a framework based on specifications of machines that ...

Keywords: binary translation, dynamic compilation, dynamic execution, emulation, interpretation

5 An unconventional proposal: using the x86 architecture as the ubiquitous



Jochen Liedtke, Nayeem Islam, Trent Jaeger, Vsevolod Panteleenko, Yoonho Park September 1998 Proceedings of the 8th ACM SIGOPS European workshop on Support for composing distributed applications EW 8

Publisher: ACM Press

Full text available: Tpdf(410.74 KB).

Additional Information: full citation, index terms

6 A dynamic binary translation approach to architectural simulation

Harold W. Cain, Kevin M. Lepak, Mikko H. Lipasti

March 2001 ACM SIGARCH Computer Architecture News, Volume 29 Issue 1

Publisher: ACM Press

Full text available: pdf(669.63 Additional Information: full citation, abstract, index terms

We present the design of a PowerPC-based simulation infrastructure for architectural research. Our infrastructure uses an execution-driven out-of-order processor timing simulator from the SimpleScalar tool set. While porting SimpleScalar to the PowerPC architecture, we would like to remain compatible with other versions of SimpleScalar. We accomplish this by performing dynamic binary translation of the PowerPC instruction set architecture to the SimpleScalar instruction set architecture, and by ...

7 Native Linux on the PowerPC

Cort Dougan

May 1997 Linux Journal

Publisher: Specialized Systems Consultants, Inc.









Full text available: html(11.24 Additional Information: full citation, abstract, references, index terms

Users of the PowerPC no longer have to settle for less--here's how to run Linux on machines with the PCI bus

8 The Parallel Protocol Engine

Matthias Kaiserswerth

December 1993 IEEE/ACM Transactions on Networking (TON), Volume 1 Issue 6

Publisher: IEEE Press

Full text available: pdf(1.65 MB) Additional Information: full citation, references, citings, index

terms, review

9 Security and protection: Packet decoding using context sensitive parsing

Sylvain Marquis, Thomas R Dean, Scott Knight

October 2006 Proceedings of the 2006 conference of the Center for Advanced Studies on Collaborative research CASCON '06

Publisher: ACM Press

Full text available: pdf(252.90

KB) (4)

Additional Information: full citation, abstract, references

htm(1.23 KB)

Protocol tester is a project at RMC and Queen's that applies program transformation techniques to protocol data to evaluate the security of network applications. As part of this process, binary protocols are translated into a textual representation. This paper describes a translation process using a context sensitive parser that eliminates the need to write custom code to decode each individual protocol. It is a template driven top down parser augmented by a constraint engine. The constraint eng ...

10 <u>Architectural exploration and system simulations: An efficient retargetable</u> framework for instruction-set simulation



Mehrdad Reshadi, Nikhil Bansal, Prabhat Mishra, Nikil Dutt

October 2003 Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis CODES+ISSS '03

Publisher: ACM Press

Full text available: pdf(251.51 Additional Information: full citation, abstract, references, citings, index terms

Instruction-set architecture (ISA) simulators are an integral part of today's processor and software design process. While increasing complexity of the architectures demands high performance simulation, the increasing variety of available architectures makes retargetability a critical feature of an instruction-set simulator. Retargetability requires generic models while high performance demands target specific customizations. To address these contradictory requirements, we have developed a gener ...

Keywords: architecture description language, decode algorithm, generic instruction model, instruction binary encoding, retargetable instruction-set simulation

11 <u>A retargetable framework for instruction-set architecture simulation</u> Mehrdad Reshadi, Nikil Dutt, Prabhat Mishra





May 2006 ACM Transactions on Embedded Computing Systems (TECS),

Volume 5 Issue 2

Publisher: ACM Press

Full text available: pdf(694.34 Additional Information: full citation, abstract, references, citings, index terms

Instruction-set architecture (ISA) simulators are an integral part of today's processor and software design process. While increasing complexity of the architectures demands high-performance simulation, the increasing variety of available architectures makes retargetability a critical feature of an instruction-set simulator. Retargetability requires generic models while high-performance demands target specific customizations. To address these contradictory requirements, we have developed a gener ...

Keywords: Retargetable instruction-set simulation, architecture description language, decode algorithm, generic instruction model, instruction binary encoding

12 Implementation aspects of a SPARC V9 complete machine simulator

Bill Clarke, Adam Czezowski, Peter Strazdins

January 2002 Australian Computer Science Communications, Proceedings of the twenty-fifth Australasian conference on Computer science -Volume 4 ACSC '02, Volume 24 Issue 1

Publisher: Australian Computer Society, Inc., IEEE Computer Society Press

Full text available: Additional Information: full citation, abstract, references, index terms

In this paper we present work in progress in the development of a complete machine simulator for the UltraSPARC, an implementation of the SPARC V9 architecture. The complexity of the UltraSPARC ISA presents many challenges in developing a reliable and yet reasonably efficient implementation of such a simulator. Our implementation includes a heavily object-oriented design for the simulator modules and infrastructure, caching of repeated computations for performance, adding an OS (system call) emu ...

Keywords: SMP, SPARC V9 ISA, UltraSPARC, complete machine simulator, execution-driven simulation, object-oriented design

13 Performance Experiments with the High Level Architecture and the Total Airport and Airspace Model (TAAM)

David J. Bodoh, Dr. Frederick Wieland

June 2003 Proceedings of the seventeenth workshop on Parallel and distributed simulation PADS '03

Publisher: IEEE Computer Society

Full text available: pdf(238.16

KB) 🗐

Additional Information: full citation, abstract, citings, index terms

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As it was originally envisioned and commonly used, theHLA is a mechanism for interconnecting disparatesimulations over a network. Its main application has beendistributed wargaming, where simulations prepared by different organizations are combined in a virtualenvironment for a specific training exercise or studyobjective. The individual simulations are called federatesin the HLA world, while the collection of federates that interoperate in the virtual world is called a federation. The HLA specifie ...

14 Retrospective: what have we learned from the PDP-11—what we have

learned from VAX and Alpha

Gorden Bell, W. D. Strecker

August 1998 25 years of the international symposia on Computer architecture (selected papers) ISCA '98

Publisher: ACM Press

Full text available: pdf(665.85 KB)

Additional Information: full citation, references, index terms

15 Features: No Source Code? No Problem!

Peter Phillips, George Phillips

September 2003 **Queue**, Volume 1 Issue 6

Publisher: ACM Press

Full text available: pdf(896.02

KB) (S)

Additional Information: full citation, abstract, index terms, review

html(24.75 KB)

What if you have to port a program, but all you have is binary?

16 Compiler technology for parallel machines: Evaluation of distributed communication systems

Ian Parsons

October 1993 Proceedings of the 1993 conference of the Centre for Advanced Studies on Collaborative research: distributed computing -Volume 2 CASCON '93

Publisher: IBM Press

Full text available: T pdf(1.04 MB) Additional Information: full citation, abstract, references, citings

Selecting a distributed communication system is a balancing act. Ease of use, efficiency of the final product, and future needs are not mutually exclusive considerations. Several questions spring to mind immediately. What are the requirements of the communication system? What is available to use? What are the requirements of the user? Software engineers desire software to have clean interfaces and to make any internal details inaccessible to the other components. Performance users want the soft ...

17 Improving the efficiency of the OSI checksum calculation



K. Sklower

October 1989 ACM SIGCOMM Computer Communication Review, Volume 19

Issue 5

Publisher: ACM Press

Full text available: pdf(629.71

Additional Information: full citation, abstract, citings, index terms

It is known that using larger byte--sizes to access memory usually results in faster computations of checksum algorithms. This paper proposes two different ways to use larger byte--sizes to improve the performance of the OSI checksum. First, an algorithm is presented that computes the 8--bit checksum using 16-bit integers. It is shown that this algorithm yields a 5 to 20 percent performance improvement on many architectures. Second, the benefits of expanding the basic computation unit of the OSI ...

18 Binary translation



Richard L. Sites, Anton Chernoff, Matthew B. Kirk, Maurice P. Marks, Scott G.

Robinson

February 1993 Communications of the ACM, Volume 36 Issue 2

Publisher: ACM Press

Full text available: pdf(4.84 MB) Additional Information: full citation, references, citings, index terms

Keywords: CISC computers, RISC computers, binary translation, computer architecture, processor architecture translation

19 Transcoding media for bandwidth constrained mobile devices

Kevin Curran, Stephen Annesley

March 2005 International Journal of Network Management, Volume 15 Issue 2

Publisher: John Wiley & Sons, Inc.

Full text available: pdf(179.00 Additional Information: full citation, abstract, references, citings, index terms

Bandwidth is an important consideration when dealing with streaming media. More bandwidth is required for complex data such as video as opposed to a simple audio file. When delivering streaming media, sufficient bandwidth is required to achieve an acceptable level of performance. If the information streamed exceeds the bandwidth capacity of the client the result will be 'choppy' and incomplete with possible loss of transmission. Transcoding typically refers to the adaptation of streaming content ...

The i860 $\frac{7M}{2}$ 64-bit supercomputing microprocessor



L. Kohn, N. Margulis

August 1989 Proceedings of the 1989 ACM/IEEE conference on Supercomputing Supercomputing '89

Publisher: ACM Press

Full text available: pdf(575.98 Additional Information: full citation, abstract, references, citings, index terms

The Intel i860TM processor is a RISC-based microprocessor incorporating a RISC core with memory management, a floating point unit, and caches on a single chip. The 1,000,000 transistors allow a single chip implementation with highly optimized interunit communication and wide internal data buses. The parallelism and pipelining between the execution units, and the innovative cache management techniques are under explicit control of software. Vectorizable applications can ...

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Endian transformation - Patent 20040204929

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Endianness in the Solaris Operating Environment

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myEndian) { putAlert(makeMessage("Tileset file [%s], unexpected endian mirror?", vtc->tilesetFileName), ALERT_CONTINUE); istat = 1; ... www.geodyssey.com/tileshare/macosxsource/viewtgxm_file.c - 17k - Cached - Similar pages

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... #ifndef QT_NO_IMAGE_MIRROR QImage mirror() const; QImage mirror(bool horizontally, bool vertically) const; #endif QImage swapRGB() const; static **Endian** ... doc.trolltech.com/3.3/qimage-h.html - 15k - <u>Cached</u> - <u>Similar pages</u>

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